REMARKS

Examiner P. Perkins is thanked for the thorough examination and search of the subject Patent Application. Claims 12 and 22 have been amended.

All Claims are believed to be in condition for Allowance and that is so requested.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 1-5, 8, 10, 12-16, and 20 as being unpatentable over Ngo et al in view of Givens et al is requested in view of Amended Claim 12 and in accordance with the following remarks.

It is agreed that the combination of Ngo et al and Givens et al teaches forming semiconductor device structures and forming copper damascene metallization. The references do not disclose the critical step in Applicants' invention of coating the deposition chamber walls with an oxide layer (e.g. Claim 1, lines 9-10 and page 7, second full paragraph). Ngo et al discusses the presence of an oxide layer on the copper surface of the wafer that they believe is formed during CMP (col. 3, lines 13-14). However, this oxide layer is not purposefully deposited onto the wafer (see 24 in Fig.

2 as contrasted with 32 in Applicants' Fig. 4). An oxide layer is not purposefully deposited onto the deposition chamber walls in Ngo et al. There is no teaching or suggestion in Ngo et al or in Givens et al or in their combination that an oxide layer be deposited onto the deposition chamber walls prior to plasma treatment and capping layer deposition.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 1-5, 8, 10, 12-16, and 20 as being unpatentable over Ngo et al in view of Givens et al is requested in view of Amended Claim 12 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 6, 9, 11, 17, 19, 21, 22-27, and 29 as being unpatentable over Ngo et al in view of Givens et al and further in view of Law et al is requested in view of Amended Claims 12 and 22 and in accordance with the following remarks.

Claims 12 and 22 have been amended to make it clear that the oxide layer is deposited both on the wafer and on the chamber walls (see the second full paragraph on page 7). As discussed above, the combination of Ngo et al and Givens et al does not teach or suggest the critical deposition of oxide

on the deposition chamber walls. This deposition prevents the capping layer from coating the chamber walls during capping layer deposition and thereby causing copper hillocks to form.

It is not agreed that Law et al discloses a method of copper metallization. As stated in the Abstract and in col. 3, lines 41-46, Law et al discloses a method of depositing amorphous silicon layers on a substrate. The topmost layer of the substrate contains a layer of patterned aluminum (col. 4, lines 37-39), not a copper damascene layer. The only mention of an oxide coating in Law et al is the mention in col. 3, lines 59-61 that the aluminum susceptor is coated with an aluminum oxide layer. This is in the description of the components of the deposition chamber, not a part of the method of depositing the amorphous silicon layers. There is no mention in Law et al that the time between copper CMP and capping layer deposition should be no longer than 24 hours. There is no mention of copper CMP in Law et al and no mention of any time frame at all.

It is not agreed that there is any motivation to combine Law et al with Ngo et al and Givens et al since Law et al is not in the field of copper metallization. Even if they are combined, there is no teaching or suggestion in Law et al

to coat the walls of the chamber with oxide or to have a time frame of less than 24 hours between any processing steps. Thus, the combination of references do not teach or suggest the critical features of Applicants' invention in which an oxide layer is coated on the walls of the deposition chamber prior to the capping layer deposition and there is a time lapse of less than 24 hours between copper CMP and capping layer deposition.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 6, 9, 11, 17, 19, 21, 22-27, and 29 as being unpatentable over Ngo et al in view of Givens et al and further in view of Law et al is requested in view of Amended Claims 12 and 22 and in accordance with the remarks above.

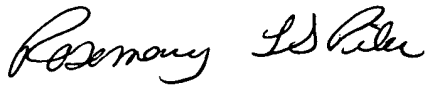
Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner Perkins not find that the Claims are now Allowable that she call the undersigned at 765 4530866 to overcome any problems

preventing allowance.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the Claims as follows:

12. (AMENDED) A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing an opening through a dielectric layer overlying a substrate on a wafer;

forming a copper layer overlying said dielectric layer and completely filling said opening;

polishing back said copper layer to leave said copper layer only within said opening;

coating an oxide layer <u>on said dielectric layer and said copper layer and</u> on the walls of a deposition chamber;

thereafter heating said wafer in said deposition chamber using NH_3 plasma; and

thereafter depositing in said deposition chamber a capping layer overlying said oxide layer to complete said copper metallization in said fabrication of said integrated circuit device.

22. (AMENDED) A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing an opening through a dielectric layer overlying a substrate on a wafer;

forming a copper layer overlying said dielectric layer and completely filling said opening;

polishing back said copper layer to leave said copper layer only within said opening; and

within 24 hours after said polishing back said copper layer, completing the following steps:

coating an oxide layer on said dielectric layer and said copper layer and on the walls of a deposition chamber;

thereafter heating in said deposition chamber said wafer using NH_3 plasma; and

thereafter depositing in said deposition chamber a capping layer overlying said oxide layer wherein said oxide layer on said walls of said deposition chamber prevents said capping layer from coating said deposition chamber walls thereby preventing formation of copper hillocks to complete said copper metallization in said fabrication of said integrated circuit device.